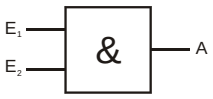
Construction of a digital counter

1 Introduction

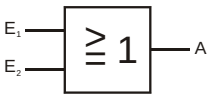
Some information can be divided into a number of dual choices (yes/no, on/off, etc.), which are designated as bit (binary digit). The binary or dual system has only two ciphers “0” and “1”, which should be understood by the presentation of numbers as the coefficients of potencies to the basis 2.
Binary signals can be processed by logical connections, whose main elements are “AND”, “OR” and “NOT”. These connections are realized in form of so-called gate as an elementary electronic circuit. Its behavior is described in connection tables (fig.1). All the other connections can be produced in a basis of main connections and combined into more complex systems. Such as: counters, computers and data processing units, etc. (The details about the electronic realization of logical connections s. Jean Pütz, “Introduction to electrical technology”, chap. 8 / K.Block “Introduction to Electronics 2”, publisher H. Stam.)

AND



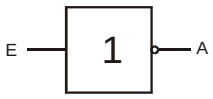
E_1	E_2	A
0	0	0
1	0	0
0	1	0
1	1	1

OR



E_1	E_2	A
0	0	0
1	0	1
0	1	1
1	1	1

NOT



E	A
0	1
1	0

fig. 1: Schematic designator and connection schemes of elementary gates.

2 Tips to the construnction

The schemes are put in a plug board. The inputs of the connections have got buttons; the outputs have got light-emitting diodes. Bright LEDs show the position “1”, dark LEDs show the position “0”. Note:

- Open inputs are always in the position „1“.
- If a schematic designator with four inputs can be found in the scheme, it should certainly be used. The same is for schematic designators with two inputs.
- In more complex appliances we should not confuse a NAND with AND: they differ only in a small circle! (just the same for OR and NOR)

The appliance is much subjected to vibration at the end of scheme! It is necessary to pay attention to the fact that the stopwatch does not start too early, i.e. that the measurement always starts exactly from 0.

3 Tasks

1. A scheme of a NAND gate (AND-series with connected NOT). A scheme of a NOR gate (OR with series-connected NOT). The inputs of connections are connected with buttons, the outputs are connected with light-emitting diodes in that case.

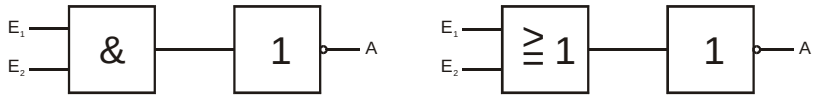


fig. 2: Here is a scheme of NAND- and NOR-gates

2. RS flip-flop is built in from two NOR-/ NAND-gates (fig. 3) and the connection table is accepted.

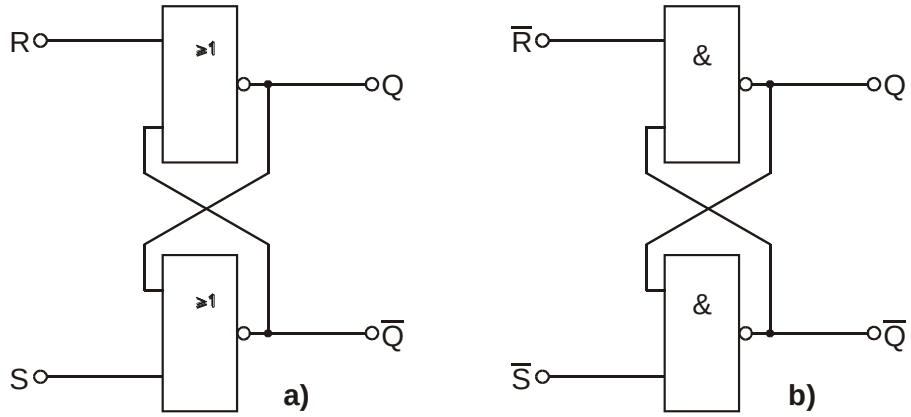


fig. 3: Here is a scheme of RS flip-flops a) from NOR- and b) from NAND-gates

Tips: the connection schemes should be accepted in the following order:

a)

R	S
1	1
1	0
0	0
0	1
0	0

b)

$\bar{R}$	$\bar{S}$
0	0
1	0
1	1
0	1
1	1

because the connection result with the input combination R = S = 0 (or $\bar{R}=1, \bar{S}=1$ with a scheme b)) depends on the previous state of the inputs. The changes at the outputs Q and $\bar{Q}$ ($\bar{Q}$ is to Q inverted output) are taken into consideration, if R or S on 1 (or $\bar{R}$ oder $\bar{S}$ on 0) is put. The input combination R = S. = 1 (or $\bar{R}=\bar{S}=0$) leads to the indefinite (=not defined) state $Q=\bar{Q}=0$ (or $Q=\bar{Q}=1$).

3. A controllable RS flip-flop keeps one (at least) other input. The logical state of this input fixes whether the information is taken or not in the Set- or Reset- input.
The presented in fig. 4 controllable flip-flops are built and the connection tables are accepted. It is necessary to use the under 2.) chosen order to be able to compare the flip-flops again, in each case for C = 0 and C = 1!

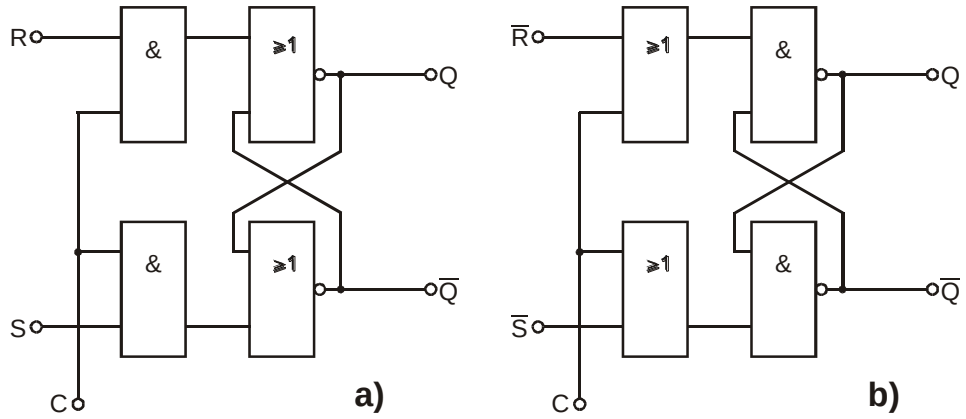


fig. 4: controllable RS flip-flops a) 1-active and b) 0-active.

4. In JK-Master-Slave-flip-flop two controllable flip-flops are switched one after another. (By additional inputs in the Slave flip-flop the outputs can be put independent of the tact in C.) The JK flip-flop from fig. 5 is built and the behavior is shown with regard to the taking of input information after a tact impulse in the form of a table. In this regard for the **input state J = K = 1** is taken the interconnection between the tact in C and the output Q in an impulse diagram. Describe the relations of the frequency in C and Q.

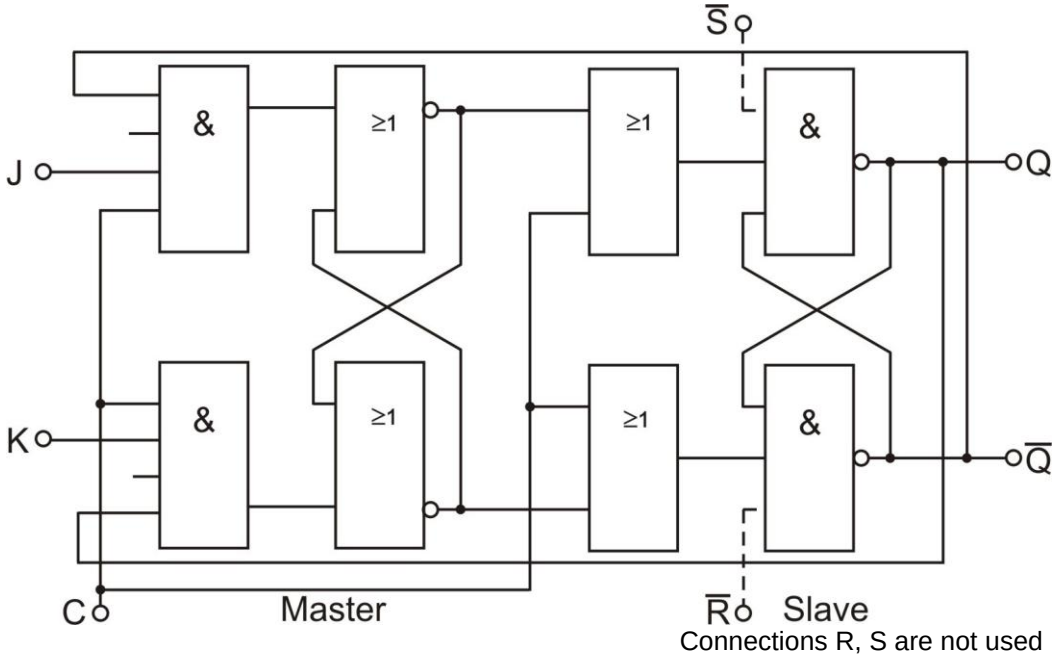


fig. 5: Tact state controllable JK-Master-Slave-flip-flop with tact independent Set/Reset-inputs.

5. A 4-bit digital counter is built from four JK flip-flops (fig. 6a) and checked for his function. In that case, use the button “single tact”! In the impulse diagram (fig. 6b) the output impulses of the single stages (depending the time) are shown. Make a translation table from decimal to binary numbers!

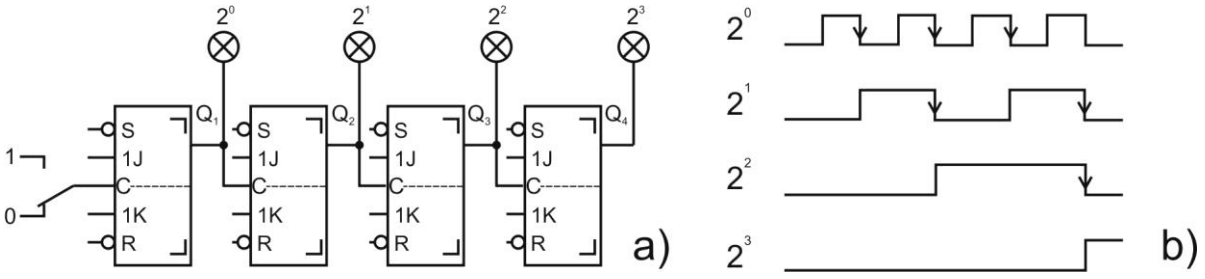


fig. 6: 4-bit binary numbers from 4 JK flip-flops, impulse diagram

6. The counter is expanded by an Overflow- announcement and used for the time measurement of a rolling ball on an inclined surface (fig. 7).

Explanation: The under 5.) overbuilt counter represents numbers from 0 to 15 in binary code. If more than 15 impulses will be counted, it could be done in principle by serial switching of following JK flip-flop. But here it is possible to use another way: The lighting of another lamp after 15 counting impulse signalizes the excess of the counting module.

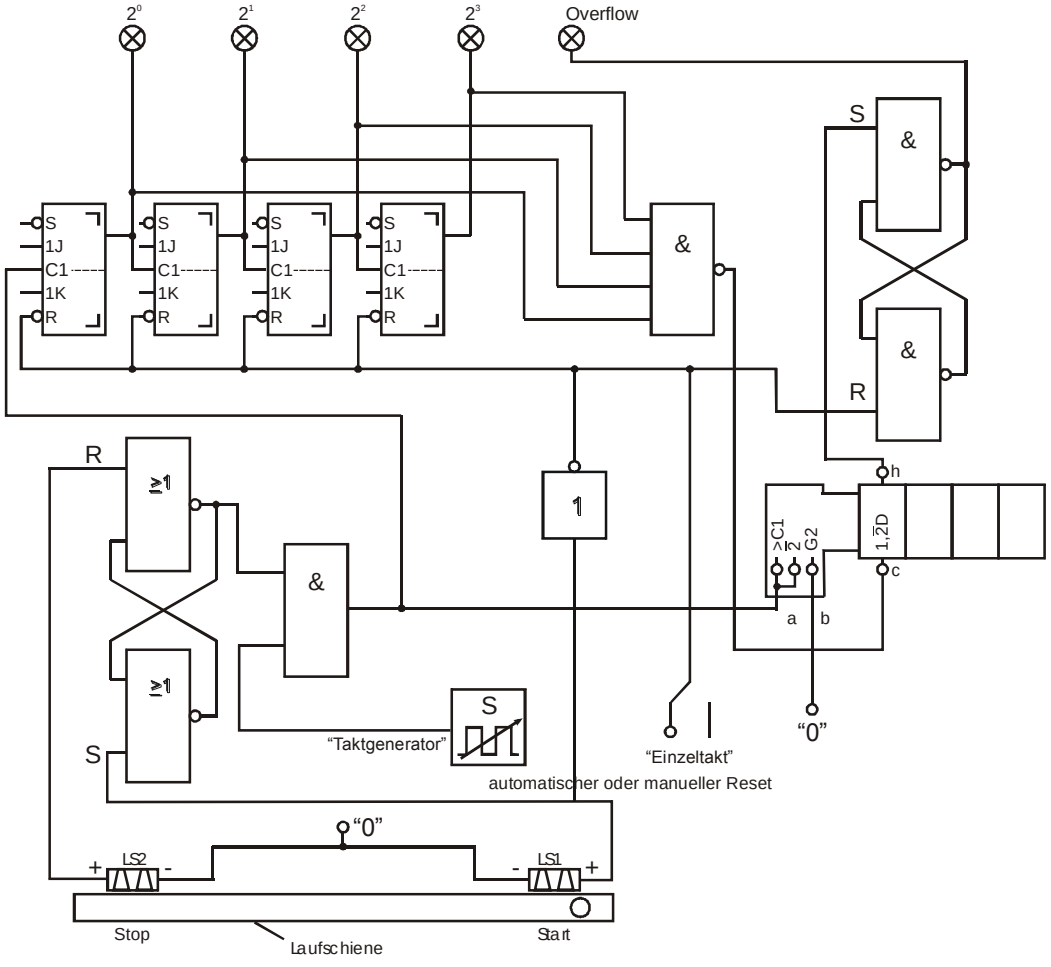


fig. 7: Digital stopwatch with regulation by light barriers

"0" appears at the output of fourfold-NAND-gate if all 4 lamps of the counter lighten (under the 15th impulse). However, the overflow-announcement is to come to light only under the 16th impulse. So the information about a shifting register is slowed by tact and puts exactly at the 16th impulse the RS flip-flop with the overflow light. The RS flip-flop can be reset with the other flip-flops together. In this way, the count area has been extended to 31. What is the disadvantage of this method?

If the counter is used as a stopwatch, the impulses of constant frequency are given to the counter input for a period of measured time. The AND-connection can only count the impulses when the RS flip-flop is set. It happens by means of the shown light barrier arrangement.
What's the difference between a manual and an automatic reset? What factors are important to become similar measurements?

The stopwatch doesn't need to be calibrated in seconds; it is enough to select the tact frequency that about 30 impulses are counted for the longest distance. By variation of the distance length, the way-time-law should be proved for a uniformly accelerated motion. Will the expected quadratic dependence be received? The use of logarithmic laws and logarithmic notation offers a more exact designation of the exponent z ($s = 1/2\ a\ t^z + v_0\ t + s_0$). The necessary conditions and the mathematical considerations must be noted. The discussion of the deviations from the expected result is highly recommended!